PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

To:
MIYAI, Teruo
P.O. Box 24 OMM Building
7-31, Otemae 1-chome
Chuo-ku
Osaka-shi
Osaka 540-6591
JAPON

Date of mailing (day/month/year)	
07 January 1999 (07.01.99)	
Applicant's or agent's file reference PM9805-PCT	**IMPORTANT NOTICE**
International application No. PCT/JP98/02544	**International filing date** (day/month/year) 08 June 1998 (08.06.98)
	Priority date (day/month/year) 27 June 1997 (27.06.97)
Applicant MATSUSHITA ELECTRONICS CORPORATION et al	

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:
   CN,EP,KR,US

   In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:
   SG

   The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on
   07 January 1999 (07.01.99) under No. WO 99/00826

REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, **a demand for international preliminary examination** must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the **national phase**, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer
J. Zahra

Telephone No. (41-22) 338.83.38

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

PCT

To:
MIYAI, Teruo
P.O. Box 24 OMM Bldg.
7-31, Otemae 1-chome, Chuo-Ku
Osaka-shi, Osaka 540
JAPON

NOTIFICATION OF RECEIPT OF DEMAND BY COMPETENT INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

(PCT Rules 59.3(e) and 61.1(b), first sentence and Administrative Instructions, Section 601(a))

Date of mailing *(day/month/year)*: 08.02.99

Applicant's or agent's file reference: PM9805-PCT

IMPORTANT NOTIFICATION

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP 98/02544	08/06/1998	27/06/1997

Applicant: MATSUSHITA ELECTRONICS CORPORATION et al.

1. The applicant is hereby **notified** that this International Preliminary Examining Authority considers the following date as the date of receipt of the demand for international preliminary examination of the international application:

07/01/1999

2. This date of receipt is:

- [x] the actual date of receipt of the demand by this Authority (Rule 61.1(b)).
- [ ] the actual date of receipt of the demand on behalf of this Authority (Rule 59.3(e)).
- [ ] the date on which this Authority has, in response to the invitation to correct defects in the demand (Form PCT/IPEA/404), received the required corrections.

3. [ ] **ATTENTION:** That date of receipt is **AFTER** the expiration of 19 months from the priority date. Consequently, the election(s) made in the demand does (do) not have the effect of postponing the entry into the national phase until 30 months from the priority date (or later in some Offices) (Article 39(1)). Therefore, the acts for entry into the national phase must be performed within 20 months from the priority date (or later in some Offices) (Article 22). For details, see the *PCT Applicant's Guide*, Volume II.

[ ] *(If applicable)* This notification confirms the information given by telephone, facsimile transmission or in person on: _____

4. Only where paragraph 3 applies, a copy of this notification has been sent to the International Bureau.

Name and mailing address of the IPEA/

European Patent Office
D-80298 Munich
Tel. (+49-89) 2399-0, Tx: 523656 epmu d
Fax: (+49-89) 2399-4465

Authorized officer: Martina Nilsson

Telephone No.: -8856

Form PCT/IPEA/402 (July 1998) P20452 (03/02/1999)

PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No.

International Filing Date

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference *(if desired) (12 characters maximum)* PM9805-PCT

Box No. I **TITLE OF INVENTION**
RESIN MOLDED TYPE SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME

Box No. II **APPLICANT**

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

Matsushita Electronics Corporation
1-1, Saiwai-cho, Takatsuki-shi, Osaka,
569-1143 JAPAN

☐ This person is also inventor.

Telephone No. 0726-82-7684

Facsimile No. 0726-82-7599

Teleprinter No.

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of: ☐ all designated States ☑ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Box No. III **FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)**

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

MINAMIO Masanori
23-8, Kamishijou-cho, Higashiosaka-shi,
Osaka, 579-8052 JAPAN

This person is:
☐ applicant only
☑ applicant and inventor
☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☑ the United States of America only ☐ the States indicated in the Supplemental Box

☑ Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV **AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE**

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: ☑ agent ☐ common representative

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

7617 Patent Attorney MIYAI Teruo
P.O.Box 24 OMM Bldg.
7-31, Otemae 1-chome, Chuo-ku,
Osaka-shi, Osaka, 540-6591 JAPAN

Telephone No. 06-943-2381

Facsimile No. 06-943-2382

Teleprinter No.

☐ Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Continuation of Box No. III FURTHER APPLICANTS AND/OR (FURTHER) INVENTORS

If none of the following sub-boxes is used, this sheet is not to be included in the request.

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

KONISHI Satoru
28-100, Hirao, Kohata, Uji-shi,
Kyoto, 611-0002 JAPAN

This person is:
- ☐ applicant only
- ☑ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☑ the United States of America only
- ☐ the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

MORISHITA Yoshihiko
39-30, Akeno-cho, Takatsuki-shi,
Osaka, 569-0082 JAPAN

This person is:
- ☐ applicant only
- ☑ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☑ the United States of America only
- ☐ the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

YAMADA Yuichiro
138-3, Hazukashi-shimizu-cho, Fushimi-ku,
Kyoto-shi, Kyoto, 612-8485 JAPAN

This person is:
- ☐ applicant only
- ☑ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☑ the United States of America only
- ☐ the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (i.e. country) of residence if no State of residence is indicated below.)*

ITOH Fumito
1-16-3, Sawarakinishi, Ibaraki-shi,
Osaka, 567-0868 JAPAN

This person is:
- ☐ applicant only
- ☑ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

State *(i.e. country)* of nationality: JAPAN

State *(i.e. country)* of residence: JAPAN

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☑ the United States of America only
- ☐ the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on another continuation sheet.

Box No.V DESIGNATION OF STATES

The following designations are hereby made under Rule 4.9(a) *(mark the applicable check-boxes; at least one must be marked)*:

Regional Patent

- ☐ **AP** **ARIPO Patent:** GH Ghana, GM Gambia, KE Kenya, LS Lesotho, MW Malawi, SD Sudan, SZ Swaziland, UG Uganda, ZW Zimbabwe, and any other State which is a Contracting State of the Harare Protocol and of the PCT
- ☐ **EA** **Eurasian Patent:** AM Armenia, AZ Azerbaijan, BY Belarus, KG Kyrgyzstan, KZ Kazakhstan, MD Republic of Moldova, RU Russian Federation, TJ Tajikistan, TM Turkmenistan, and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT
- ☑ **EP** **European Patent:** AT Austria, BE Belgium, CH and LI Switzerland and Liechtenstein, DE Germany, DK Denmark, ES Spain, FI Finland, FR France, GB United Kingdom, GR Greece, IE Ireland, IT Italy, LU Luxembourg, MC Monaco, NL Netherlands, PT Portugal, SE Sweden, and any other State which is a Contracting State of the European Patent Convention and of the PCT
- ☐ **OA** **OAPI Patent:** BF Burkina Faso, BJ Benin, CF Central African Republic, CG Congo, CI Côte d'Ivoire, CM Cameroon, GA Gabon, GN Guinea, ML Mali, MR Mauritania, NE Niger, SN Senegal, TD Chad, TG Togo, and any other State which is a member State of OAPI and a Contracting State of the PCT *(if other kind of protection or treatment desired, specify on dotted line)* .....

National Patent *(if other kind of protection or treatment desired, specify on dotted line)*:

- ☐ **AL** Albania .....
- ☐ **AM** Armenia .....
- ☐ **AT** Austria .....
- ☐ **AU** Australia .....
- ☐ **AZ** Azerbaijan
- ☐ **BA** Bosnia and Herzegovina .....
- ☐ **BB** Barbados
- ☐ **BG** Bulgaria .....
- ☐ **BR** Brazil .....
- ☐ **BY** Belarus
- ☐ **CA** Canada
- ☐ **CH and LI** Switzerland and Liechtenstein
- ☑ **CN** China .....
- ☐ **CU** Cuba .....
- ☐ **CZ** Czech Republic .....
- ☐ **DE** Germany .....
- ☐ **DK** Denmark .....
- ☐ **EE** Estonia .....
- ☐ **ES** Spain .....
- ☐ **FI** Finland .....
- ☐ **GB** United Kingdom
- ☐ **GE** Georgia .....
- ☐ **GH** Ghana .....
- ☐ **GM** Gambia
- ☐ **GW** Guinea-Bissau .....
- ☐ **HU** Hungary .....
- ☐ **ID** Indonesia
- ☐ **IL** Israel .....
- ☐ **IS** Iceland
- ☐ **JP** Japan .....
- ☐ **KE** Kenya .....
- ☐ **KG** Kyrgyzstan .....
- ☐ **KP** Democratic People's Republic of Korea .....
- ☑ **KR** Republic of Korea .....
- ☐ **KZ** Kazakhstan .....
- ☐ **LC** Saint Lucia
- ☐ **LK** Sri Lanka
- ☐ **LR** Liberia
- ☐ **LS** Lesotho .....
- ☐ **LT** Lithuania
- ☐ **LU** Luxembourg
- ☐ **LV** Latvia
- ☐ **MD** Republic of Moldova .....
- ☐ **MG** Madagascar .....
- ☐ **MK** The former Yugoslav Republic of Macedonia .....
- ☐ **MN** Mongolia
- ☐ **MW** Malawi .....
- ☐ **MX** Mexico .....
- ☐ **NO** Norway
- ☐ **NZ** New Zealand .....
- ☐ **PL** Poland .....
- ☐ **PT** Portugal .....
- ☐ **RO** Romania
- ☐ **RU** Russian Federation .....
- ☐ **SD** Sudan
- ☐ **SE** Sweden
- ☑ **SG** Singapore
- ☐ **SI** Slovenia .....
- ☐ **SK** Slovakia .....
- ☐ **SL** Sierra Leone
- ☐ **TJ** Tajikistan .....
- ☐ **TM** Turkmenistan .....
- ☐ **TR** Turkey .....
- ☐ **TT** Trinidad and Tobago .....
- ☐ **UA** Ukraine .....
- ☐ **UG** Uganda .....
- ☑ **US** United States of America .....
- ☐ **UZ** Uzbekistan .....
- ☐ **VN** Viet Nam .....
- ☐ **YU** Yugoslavia .....
- ☐ **ZW** Zimbabwe .....

Check-boxes reserved for designating States (for the purposes of a national patent) which have become party to the PCT after issuance of this sheet:

- ☐ .....
- ☐ .....
- ☐ .....

In addition to the designations made above, the applicant also makes under Rule 4.9(b) all designations which would be permitted under the PCT except the designation(s) of _____.

The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. *(Confirmation of a designation consists of the filing of a notice specifying that designation and the payment of the designation and confirmation fees. Confirmation must reach the receiving Office within the 15-month time limit.)*

Box No. VI PRIORITY CLAIM Further priority claims are indicated in the Supplemental Box ☐

The priority of the following earlier application(s) is hereby claimed:

Country *(in which, or for which, the application was filed)*	Filing Date *(day/month/year)*	Application No.	Office of filing *(only for regional or international application)*
item (1) JAPAN	27. 06. 97	Patent Application 9-171395	
item (2) JAPAN	23. 03. 98	Patent Application 10-073711	
item (3)			

Mark the following check-box if the certified copy of the earlier application is to be issued by the Office which for the purposes of the present international application is the receiving Office (a fee may be required):

☐ The receiving Office is hereby requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) identified above as item(s) : _____

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(If two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used):* ISA / EP

Earlier search *Fill in where a search (international, international-type or other) by the International Searching Authority has already been carried out or requested and the Authority is now requested to base the international search, to the extent possible, on the results of that earlier search. Identify such search or request either by reference to the relevant application (or the translation thereof) or by reference to the search request:*

Country (or regional Office): Date *(day/month/year)*: Number:

Box No. VIII CHECK LIST

This international application contains the following number of sheets:

1. request	:	4 sheets
2. description	:	23 sheets
3. claims	:	6 sheets
4. abstract	:	1 sheets
5. drawings	:	6 sheets
Total	:	40 sheets

This international application is accompanied by the item(s) marked below:

1. ☑ separate signed power of attorney
2. ☐ copy of general power of attorney
3. ☐ statement explaining lack of signature
4. ☐ priority document(s) *identified in Box No. VI as item(s):*
5. ☐ fee calculation sheet
6. ☐ separate indications concerning deposited microorganisms
7. ☐ nucleotide and/or amino acid sequence listing (diskette)
8. ☐ other *(specify)*:

Figure No. 1 of the drawings (if any) should accompany the abstract when it is published.

Box No. IX SIGNATURE OF APPLICANT OR AGENT

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request).

Miyai Teruo

MIYAI Teruo

For receiving Office use only

1. Date of actual receipt of the purported international application:
2. Drawings: ☐ received: ☐ not received:
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:
4. Date of timely receipt of the required corrections under PCT Article 11(2):
5. International Searching Authority specified by the applicant: ISA /
6. ☐ Transmittal of search copy delayed until search fee is paid

For International Bureau use only

Date of receipt of the record copy by the International Bureau:

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 98/02544

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/31

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 009, no. 230 (E-343), 17 September 1985 -& JP 60 086851 A (NIPPON DENKI KK), 16 May 1985 see abstract; figures 3,5 ---	1,7,8
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 307 (E-1229), 7 July 1992 -& JP 04 085952 A (FUJITSU LTD), 18 March 1992 see abstract; figures 1-4 --- -/--	1,7,8

[X] Further documents are listed in the continuation of box C.

[ ] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 February 1999	19. 03. 1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Zeisler, P

3

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 489 (E-0994), 24 October 1990 -& JP 02 201946 A (NEC IC MICROCOMPUT SYST LTD), 10 August 1990 see abstract	1,7,8
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 078 (E-718), 22 February 1989 -& JP 63 258050 A (MITSUBISHI ELECTRIC CORP), 25 October 1988	1
A	see abstract	8
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 346 (E-798), 3 August 1989 -& JP 01 106456 A (MATSUSHITA ELECTRIC IND CO LTD), 24 April 1989	4,5,9
A	see abstract; figures 1-3	10
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 346 (E-798), 3 August 1989 -& JP 01 106455 A (MATSUSHITA ELECTRIC IND CO LTD), 24 April 1989	2
A	see abstract; figure 1	9
X	PATENT ABSTRACTS OF JAPAN vol. 017, no. 504 (E-1430), 10 September 1993 -& JP 05 129473 A (SONY CORP), 25 May 1993	3
A	see abstract; figures 5C,5D	9,10
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 287 (E-643), 5 August 1988 -& JP 63 064351 A (TOSHIBA CORP), 22 March 1988 see abstract	2,3,5,6, 9,10
A	PATENT ABSTRACTS OF JAPAN vol. 010, no. 137 (E-405), 21 May 1986 -& JP 61 001042 A (TOSHIBA KK), 7 January 1986 see abstract	2,3,5,9, 10
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 444 (E-1265), 16 September 1992 -& JP 04 155854 A (HITACHI LTD;OTHERS: 01), 28 May 1992 see abstract	3,6,10

3

Serial Number 292530008 Dispatch Number 193474

Dispatch Date Dec. 22, 1998

Notice of Reasons for Rejection

Patent Application No.	10-073711
Drafting Date	Dec. 10, 1998
Examiner of JPO	Eiichi TANAKA 9539 4E00
Representative/Applicant	Teruo MIYAI
Applied provision	Patent Low Section 29(1), 29(2)

This application should be refused for the reason mentioned below. If the applicant has any argument against the reason, such argument should be submitted within 60 days from the date on which this notification was dispatched.

1. The inventions in the claims listed below of the subject application should not be granted a patent under the provision of Patent Law Section 29(1)(iii) since they are inventions described in the publications listed below which were distributed in Japan or foreign countries prior to the filing of the subject application.

2. The inventions in the claims listed below of the subject application should not be granted a patent under the provision of Patent Law Section 29(2) since it could have easily been made by persons who have common knowledge in the

Continued

Continuing from the prior page

technical filed to which the inventions pertains, on the basis of the inventions described in the publications listed below which was distribted in Japan or foreign countries prior to the filling of the subject application.

Note (The list of cited documents etc. is shown below.)

<With respect to reason 1>

- Claims 1, 7, and 8
- Cited document 1
- Remark

Cited document 1 discloses a semiconductor device that is configured so that a pedestal 1 on which an integrated circuit element 5 is placed is positioned so as to be higher than the bottom face of a mold 7, and a lead portion is exposed from the mold 7 through an external bottom face (see Fig. 4).

<With respect to reason 2>

- Claims 1 to 3, 7, and 8
- Cited documents 1 and 2
- Remark

Cited document 2 discloses a semiconductor device in which plural grooves are disposed in the vicinity of a bonding portion 9 of an inner lead portion (see Fig. 1).

Continued

Continuing from the prior page

- Claims 4 to 7, 9, and 10
- Cited documents 1 to 3
- Remark

Cited document 3 discloses a lead frame in which a wider portion is disposed in a tip end portion of an inner lead. Therefore, the inventions in claims 4 to 7, 9, and 10 are mere combinations of the inventions described in cited documents 1 to 3.

The list of cited documents, etc.

1. Microfilm of Japanese Utility Model application No. SHO53-2259 (Japanese Utility Model publication (Kokai) No. SHO54-106776)
2. Microfilm of Japanese Utility Model application No. SHO59-127828 (Japanese Utility Model publication (Kokai) No. SHO61-42856)
3. Japanese Patent Publication (Kokai) No. HEI6-104364

Record of the result of prior art search

- Technical field to be searched Int. Cl(6) H01L23/50

This record is not a component of the reasons for refusal.

Any inquiry about this notification should be

addressed to:

TANAKA Eiichi, Examiner of Examination 4th Dept.

Tel. 03-3581-1101 Ext. 3425 to 3427

電産 3半

整理番号　２９２５３０００１２　発送番号　１９３４７４

発送日　平成１０年１２月２２日　1／ 2

拒絶理由通知書

2/19

特許出願の番号	平成１０年　特許願　第０７３７１１号
起案日	平成１０年１２月１０日
特許庁審査官	田中　永一　９５３９　４Ｅ００
特許出願人代理人	宮井　暎夫　殿
適用条文	第２９条第１項、第２９条第２項

この出願は、次の理由によって拒絶をすべきものである。これについて意見があれば、この通知書の発送の日から６０日以内に意見書を提出されたい。

理　由

１．この出願の下記の請求項に係る発明は、その出願前日本国内又は外国において頒布された下記の刊行物に記載された発明であるから、特許法第２９条第１項第３号に該当し、特許を受けることができない。

２．この出願の下記の請求項に係る発明は、その出願前日本国内又は外国において頒布された下記の刊行物に記載された発明に基いて、その出願前にその発明の属する技術の分野における通常の知識を有する者が容易に発明をすることができたものであるから、特許法第２９条第２項の規定により特許を受けることができない。

記　　（引用文献等については引用文献等一覧参照）

＜理由１について＞

・請求項　１、７、８

・引用文献等　１

・備考

続葉有

続　葉

引用文献１には、集積回路素子５が載置された台部１がモールド７の底面より高い位置になるように構成され、リード部がモールド７から外部底面に露出するように設けられた半導体装置が記載されている（第４図参照）。

＜理由２について＞
・請求項　１－３、７、８
・引用文献等　１－２
・備考
引用文献２には、インナーリード部のボンディング部９の近傍に複数の溝を設けた半導体装置が記載されている（第１図参照）。

・請求項　４－７、９、１０
・引用文献等　１－３
・備考
引用文献３には、インナーリードの先端部に幅の広い部分を設けたリードフレームが記載されている。よって、本願の請求項４乃至７、９並びに１０に係る発明は、引用文献１乃至３に記載された発明を単に組み合わせたものにすぎない。

引　用　文　献　等　一　覧

１．実願昭５３－２２５９号（実開昭５４－１０６７７６号）のマイクロフィルム
２．実願昭５９－１２７８２８号（実開昭６１－４２８５６号）のマイクロフィルム
３．特開平６－１０４３６４号公報

先行技術文献調査結果の記録

・調査した分野　　ＩＰＣ第６版　H01L23/50

この先行技術文献調査結果の記録は、拒絶理由を構成するものではない。

この拒絶理由通知書の内容に関する問い合わせ先
審査第四部金属加工　　審査官　田中　永一
電話　０３－３５８１－１１０１　内線　３４２５～３４２７

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 19 January 2000 (19.01.00)	
International application No. PCT/JP98/02544	**Applicant's or agent's file reference** PM9805-PCT
International filing date (day/month/year) 08 June 1998 (08.06.98)	**Priority date** (day/month/year) 27 June 1997 (27.06.97)
Applicant MINAMIO, Masanori et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

11 January 1999 (11.01.99)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer Antonia Muller
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

The demand must be filed directly with the competent International Preliminary Examining Authority or, if two or more Authorities are competent, with the one chosen by the applicant. The full name or two-letter code of that Authority may be indicated by the applicant on the line below:

IPEA/ EP

PCT

CHAPTER II

DEMAND

under Article 31 of the Patent Cooperation Treaty:
The undersigned requests that the international application specified below be the subject of international preliminary examination according to the Patent Cooperation Treaty and hereby elects all eligible States (except where otherwise indicated).

For International Preliminary Examining Authority use only

Identification of IPEA	Date of receipt of DEMAND

Box No. I IDENTIFICATION OF THE INTERNATIONAL APPLICATION

Applicant's or agent's file reference: PM9805-PCT

International application No.	International filing date *(day/month/year)*	(Earliest) Priority date *(day/month/year)*
PCT/JP98/02544	08. 06. 98	27. 06. 97

Title of invention: RESIN MOLDED TYPE SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME

Box No. II APPLICANT(S)

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

Matsushita Electronics Corporation
1-1, Saiwai-cho, Takatsuki-shi, Osaka,
569-1143 JAPAN

Telephone No.: 0726-82-7684
Facsimile No.: 0726-82-7599
Teleprinter No.:

State *(that is, country)* of nationality: JAPAN
State *(that is, country)* of residence: JAPAN

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

MINAMIO Masanori
23-8, Kamishijou-cho, Higashiosaka-shi,
Osaka, 579-8052 JAPAN

State *(that is, country)* of nationality: JAPAN
State *(that is, country)* of residence: JAPAN

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KONISHI Satoru
28-100, Hirao, Kohata, Uji-shi,
Kyoto, 611-0002 JAPAN

State *(that is, country)* of nationality: JAPAN
State *(that is, country)* of residence: JAPAN

☑ Further applicants are indicated on a continuation sheet.

Sheet No. 2

International application No.
PCT/JP98/02544

Continuation of Box No. II APPLICANT(S)

If none of the following sub-boxes is used, this sheet should not be included in the demand.

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

MORISHITA Yoshihiko
39-30, Akeno-cho, Takatsuki-shi,
Osaka, 569-0082 JAPAN

State *(that is, country)* of nationality:	State *(that is, country)* of residence:
JAPAN	JAPAN

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

YAMADA Yuichiro
138-3, Hazukashi-shimizu-cho, Fushimi-ku,
Kyoto-shi, Kyoto, 612-8485 JAPAN

State *(that is, country)* of nationality:	State *(that is, country)* of residence:
JAPAN	JAPAN

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

ITOH Fumito
1-16-3, Sawarakinishi, Ibaraki-shi,
Osaka, 567-0868 JAPAN

State *(that is, country)* of nationality:	State *(that is, country)* of residence:
JAPAN	JAPAN

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

State *(that is, country)* of nationality:	State *(that is, country)* of residence:

☐ Further applicants are indicated on another continuation sheet.

Sheet No. 3

International application No.
PCT/JP98/02544

Box No. III AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The following person is ☑ agent ☐ common representative

and ☑ has been appointed earlier and represents the applicant(s) also for international preliminary examination.

☐ is hereby appointed and any earlier appointment of (an) agent(s)/common representative is hereby revoked.

☐ is hereby appointed, specifically for the procedure before the International Preliminary Examining Authority, in addition to the agent(s)/common representative appointed earlier.

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

7617 Patent Attorney MIYAI Teruo
P.O.Box 24 OMM Bldg.
7-31, Otemae 1-chome, Chuo-ku,
Osaka-shi, Osaka, 540-6591 JAPAN

Telephone No.: 06-6943-2381

Facsimile No.: 06-6943-2382

Teleprinter No.:

☐ **Address for correspondence:** Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Box No. IV BASIS FOR INTERNATIONAL PRELIMINARY EXAMINATION

Statement concerning amendments:*

1. The applicant wishes the international preliminary examination to start on the basis of:

☑ the international application as originally filed

the description
☐ as originally filed
☐ as amended under Article 34

the claims
☐ as originally filed
☐ as amended under Article 19 (together with any accompanying statement)
☐ as amended under Article 34

the drawings
☐ as originally filed
☐ as amended under Article 34

2. ☐ The applicant wishes any amendment to the claims under Article 19 to be considered as reversed.

3. ☐ The applicant wishes the start of the international preliminary examination to be postponed until the expiration of 20 months from the priority date unless the International Preliminary Examining Authority receives a copy of any amendments made under Article 19 or a notice from the applicant that he does not wish to make such amendments (Rule 69.1(d)). *(This check-box may be marked only where the time limit under Article 19 has not yet expired.)*

* Where no check-box is marked, international preliminary examination will start on the basis of the international application as originally filed or, where a copy of amendments to the claims under Article 19 and/or amendments of the international application under Article 34 are received by the International Preliminary Examining Authority before it has begun to draw up a written opinion or the international preliminary examination report, as so amended.

Language for the purposes of international preliminary examination: English

☑ which is the language in which the international application was filed.
☐ which is the language of a translation furnished for the purposes of international search.
☐ which is the language of publication of the international application.
☐ which is the language of the translation (to be) furnished for the purposes of international preliminary examination.

Box No. V ELECTION OF STATES

The applicant hereby elects all eligible States *(that is, all States which have been designated and which are bound by Chapter II of the PCT)*

excluding the following States which the applicant wishes not to elect:

International application No.
PCT/JP98/02544

Box No. VI CHECK LIST

The demand is accompanied by the following elements, in the language referred to in Box No. IV, for the purposes of international preliminary examination:

			For International Preliminary Examining Authority use only: received	not received
1. translation of international application	:	sheets	☐	☐
2. amendments under Article 34	:	sheets	☐	☐
3. copy (or, where required, translation) of amendments under Article 19	:	sheets	☐	☐
4. copy (or, where required, translation) of statement under Article 19	:	sheets	☐	☐
5. letter	:	sheets	☐	☐
6. other *(specify)*	:	sheets	☐	☐

The demand is also accompanied by the item(s) marked below:

1. ☑ fee calculation sheet
2. ☐ separate signed power of attorney
3. ☐ copy of general power of attorney; reference number, if any:
4. ☐ statement explaining lack of signature
5. ☐ nucleotide and or amino acid sequence listing in computer readable form
6. ☑ other *(specify)*: Application for remittance & Statement of remittance

Box No. VII SIGNATURE OF APPLICANT, AGENT OR COMMON REPRESENTATIVE

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the demand).

Miyai Teruo

MIYAI Teruo

For International Preliminary Examining Authority use only

1. Date of actual receipt of DEMAND:
2. Adjusted date of receipt of demand due to CORRECTIONS under Rule 60.1(b):
3. ☐ The date of receipt of the demand is AFTER the expiration of 19 months from the priority date and item 4 or 5, below, does not apply. ☐ The applicant has been informed accordingly.
4. ☐ The date of receipt of the demand is WITHIN the period of 19 months from the priority date as extended by virtue of Rule 80.5.
5. ☐ Although the date of receipt of the demand is after the expiration of 19 months from the priority date, the delay in arrival is EXCUSED pursuant to Rule 82.

For International Bureau use only

Demand received from IPEA on:

See Notes to the demand form

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
PM9805-PCT		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP98/02544	08/06/1998	27/06/1997
International Patent Classification (IPC) or national classification and IPC H01L23/31		
Applicant MATSUSHITA ELECTRONICS CORPORATION et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 8 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
07/01/1999	19. 10. 99
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Cortes Rosa, Joao Telephone No. +49 89 2399 2264

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/JP98/02544

I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-23 as originally filed

Claims, No.:

1-10 as originally filed

Drawings, sheets:

1/6-6/6 as originally filed

2. The amendments have resulted in the cancellation of:

☐ the description, pages:
☐ the claims, Nos.:
☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	6,10
	No:	Claims	1-5,7-9
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-10
Industrial applicability (IA)	Yes:	Claims	1-10
	No:	Claims	

2. Citations and explanations

see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V

Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following documents:

D1: PATENT ABSTRACTS OF JAPAN vol. 009, no. 230 (E-343), 17 September 1985 -& JP 60 086851 A (NIPPON DENKI KK), 16 May 1985

D2: PATENT ABSTRACTS OF JAPAN vol. 016, no. 307 (E-1229), 7 July 1992 -& JP 04 085952 A (FUJITSU LTD), 18 March 1992

D3: JP 01 106455 A (MATSUSHITA ELECTRIC IND CO LTD), 24 April 1989 & the corresponding Patent Abstract of Japan

D4: PATENT ABSTRACTS OF JAPAN vol. 017, no. 504 (E-1430), 10 September 1993 -& JP 05 129473 A (SONY CORP), 25 May 1993

D5: JP 01 106456 A (MATSUSHITA ELECTRIC IND CO LTD), 24 April 1989 & the corresponding Patent Abstract of Japan

It is noted that in the International Search Report the Patent Abstracts of Japan above cited as D3 and D5 both have the same numbering, mistakenly.

A. First invention (claims 1, 7 and 8)

A.1. The subject-matter of claims 1, 7 and 8 is not new in the sense of Article 33(2) PCT.

A.1.1 Document D1 (see the Abstract) discloses a resin molded type semiconductor device comprising:
a semiconductor chip (1) which is mounted on a die pad portion (2) of a lead frame; thin metal wires (4) which electrically connect terminals of an upper face of said semiconductor chip (1) to inner portions of leads (3) of the lead frame;

a sealing resin (5) which seals an outer peripheral region of said semiconductor chip (1), said region including a thin metal wire region of the upper face of said semiconductor chip, and a lower region of said die pad portion;
and outer portions of leads (3) of the lead frame which are arranged in a bottom face region of said sealing resin, and
comprising the further feature that said die pad portion (2) is located at a position higher than said inner portions of leads (3).
The subject-matter of claim 1 does not differ therefrom.
Moreover, document D2 (see the Abstracts and in particular the Figures thereon) also discloses a semiconductor chip from which the subject-matter of claim 1 does not differ.

A.1.2. The additional features of claim 7 are known from both of D1 (see the Abstract) and D2 (see the Abstract).

A.1.3. The method defined in independent claim 8 is implicitly known from both of D1 (see the Abstract) and D2 (see the Abstract).

B. Second invention (claims 2, 3 and 9)

B.1. The subject-matter of claims 2, 3 and 9 is not new in the sense of Article 33(2) PCT.

B.1.1. Document D3 (see the Abstract) discloses a resin molded type semiconductor device comprising:
a semiconductor chip (4) which is mounted on a die pad portion of a lead frame; thin metal wires (5) which electrically connect terminals of an upper face of said semiconductor chip (4) to inner lead portions of said lead frame;
a sealing resin (6) which seals an outer peripheral region of said semiconductor chip (4), said region including a thin metal wire region of the upper face of said semiconductor chip;
and outer lead portions which are arranged in a bottom face region of said sealing resin and which are formed to be continuous to respective inner lead

portions,
comprising the further feature that at least one groove portion (2) is formed in a surface of each of said inner lead portions.
The subject-matter of claim 2 does not differ therefrom.

B.1.2. The subject-matter of independent claim 3 is known from D4 (see the Abstract and Figures 5C and 5D of the JP-document).

B.1.3. The subject-matter of independent claim 9 is known from D5 (see the Abstract and the Figures of the JP-document).

C. Third invention (claims 4, 5, 6 and 10)

C.1. The subject-matter of claims 4 and 5 is not new in the sense of Article 33(2) PCT.

C.1.1. Document D5 (see the Abstract and the Figures of the JP-document) discloses a resin molded type semiconductor device comprising:
a semiconductor chip (16) which is mounted on a die pad portion (11) of a lead frame; thin metal wires (17) which electrically connect terminals of an upper face of said semiconductor chip (16) to inner portions of leads (12) of said lead frame;
a sealing resin (18) which seals an outer peripheral region of said semiconductor chip (16), said region including a thin metal wire region of the upper face of said semiconductor chip;
and outer portions of leads (12) which are arranged in a bottom face region of said sealing resin (18) and which are formed to be continuous to respective inner portions of leads (12), and comprising the further features that
a widened portion is formed in each of said inner portions of leads (12).
The subject-matter of claim 4 does not differ therefrom.

C.1.2. The subject-matter of independent claim 5 is known from D5 (see the Abstract and the Figures of the JP-document).

C.2. The subject-matter of claims 6 and 10 does not involve an inventive step in the sense of Article 33(3) PCT.

C.2.1. The subject-matter of independent claim 6 is known from D5 (see the Abstract and the Figures of the JP-document), except the features that "a plurality of groove portions is formed in a surface" and "connecting portions of said thin metal wires on a side of said inner lead portion are disposed between said groove portions". However, since the technical meaning of forming a plurality of groove portions in just any surface of the device is not apparent (see Re Item VIII, section C.3. below) it appears that the inclusion of the features above would be merely a non-inventive design possibility.

C.2.2. Claim 10 defines a method not including any inventive process steps and not leading to a device which could be considered as inventive over the prior art devices defined in D1-D5. Therefore, the subject-matter of independent claim 10 cannot be considered as involving any inventive skill.

Re Item VIII
Certain observations on the international application

A. First invention (claims 1, 7 and 8)

A.1. The application does not meet the requirements of Article 6 PCT, because claim 1 is not clear: The feature "said lead frame is subjected to an upsetting process" is a pure method-feature and therefore not suitable to characterize a manufactured device as defined in claim 1. Therefore, said feature renders the subject-matter of said claim unclear.

B. Second invention (claims 2, 3 and 9)

B.1. The drafting of two independent device-claims (2 and 3) is not concise and renders those device-claims unclear (Article 6 PCT): It is not apparent from

the various combinations of features given thereon what the basic principle of the invention actually is. For the sake of completeness it is noted that a set of claims defining the relevant subject-matter in terms of a single independent device-claim followed by dependent claims covering features which are merely optional would rather appear appropriate.

C. Third invention (claims 4, 5, 6 and 10)

C.1. The drafting of three independent device-claims (4, 5 and 6) is not concise and renders those device-claims unclear (Article 6 PCT): It is not apparent from the various combinations of features given thereon what the basic principle of the invention actually is. For the sake of completeness it is noted that a set of claims defining the relevant subject-matter in terms of a single independent device-claim followed by dependent claims covering features which are merely optional would rather appear appropriate.

C.2. The feature of claim 5 that "at least one groove portion is formed in a surface" is not understandable, because it is not apparent which could be the technical meaning of forming such a groove portion on just any surface of the device.

C.3. The feature of claim 6 that "a plurality of groove portions is formed in a surface" is not understandable, because it is not apparent which could be the technical meaning of forming a plurality of groove portions on just any surface of the device.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L

A2

(11) International Publication Number: **WO 99/00826**

(43) International Publication Date: 7 January 1999 (07.01.99)

(21) International Application Number: PCT/JP98/02544

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(30) Priority Data:
9/171395 27 June 1997 (27.06.97) JP
10/73711 23 March 1998 (23.03.98) JP

(71) Applicant *(for all designated States except US)*: MATSUSHITA ELECTRONICS CORPORATION [JP/JP]; 1-1, Saiwai-cho, Takatsuki-shi, Osaka 569-1143 (JP).

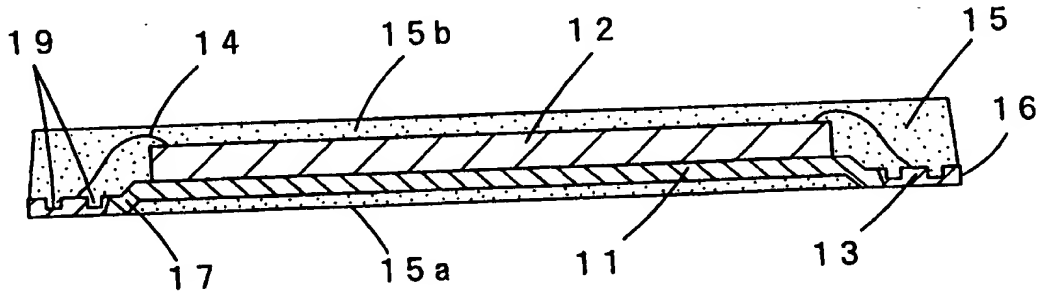
(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: MINAMIO, Masanori [JP/JP]; 23-8, Kamishijou-cho, Higashiosaka-shi, Osaka 579-8052 (JP). KONISHI, Satoru [JP/JP]; 28-100, Hirao, Kohata, Uji-shi, Kyoto 611-0002 (JP). MORISHITA, Yoshihiko [JP/JP]; 39-30, Akeno-cho, Takatsuki-shi, Osaka 569-0082 (JP). YAMADA, Yuichiro [JP/JP]; 138-3, Hazukashi-shimizu-cho, Fushimi-ku, Kyoto-shi, Kyoto 612-8485 (JP). ITOH, Fumito [JP/JP]; 1-16-3, Sawarakinishi, Ibaraki-shi, Osaka 567-0868 (JP).

(74) Agent: MIYAI, Teruo; P.O. Box 24 OMM Building, 7-31, Otemae 1-chome, Chuo-ku, Osaka-shi, Osaka 540-6591 (JP).

(81) Designated States: CN, KR, SG, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: RESIN MOLDED TYPE SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME



(57) Abstract

A resin molded type semiconductor device has: a semiconductor chip (12) which is mounted on a die pad portion (11) of a lead frame (9); thin metal wires (14) which connect terminals of the semiconductor chip (12) to inner lead portions (13) of the lead frame (9); and a sealing resin (15), and the lead frame (9) is subjected to an upsetting process so that a supporting portion (11) is located at a position higher than the inner lead portions (13). Since the sealing resin of a thickness corresponding to the step difference of the upsetting exists below the supporting portion, the adhesiveness between the lead frame and the sealing resin can be improved, and high reliability and thinning are realized. Since at least one groove portion is disposed in the surface of each of the inner lead portions (13), the anchoring effect to the sealing resin (15), stress acting on a lead portion of a product, and stress to the thin metal wires (14) can be relaxed, and leads and the thin metal wires can be prevented from peeling off.

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ML	Mali
MN	Mongolia
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RESIN MOLDED TYPE SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME

Technical Field

The invention relates to a resin molded type semiconductor device in which a semiconductor chip is mounted on a lead frame and the outer periphery of the semiconductor chip, particularly, the upper face of the semiconductor chip is molded by a sealing resin, and also to a method of manufacturing the semiconductor device.

Background Art

Recently, as the density of board mounting advances, semiconductor products which are to be mounted on a board are requested to be miniaturized and thinned. In order to realize miniaturization and thinning, the TAB mounting technique using a resin tape has been developed. In a development of a thin semiconductor product using a lead frame, a resin molded type semiconductor device of the single-side molding type in which a semiconductor chip is mounted on a lead frame and the mounting face is molded by a sealing resin has been developed.

Hereinafter, a resin molded type semiconductor device of the prior art will be described. Fig. 5 is a section view showing

a resin molded type semiconductor device of the prior art.

In the resin molded type semiconductor device of the prior art shown in Fig. 5, a semiconductor chip 3 is mounted on a die pad portion 2 of a lead frame 1, and terminals (not shown) of the semiconductor chip 3 are electrically connected to inner lead portions 4 of the lead frame 1 by thin metal wires 5. In a single face of the lead frame 1, i.e., the face of the lead frame 1 on which the semiconductor chip 3 is mounted, the outer peripheral region of the semiconductor chip 3 is molded by a sealing resin 6.

In a resin molded type semiconductor device produced so as to have a structure such as shown in Fig. 5 is provided with a structure in which an outer lead portion 7 serving as external terminals is arranged on a bottom face of the semiconductor device. Since only the face of the lead frame 1 on which the semiconductor chip 3 is mounted is molded by the sealing resin 6 and the rear face of the lead frame 1 is not substantially molded, it is possible to realize a thin resin molded type semiconductor device.

Next, in a method of manufacturing the resin molded type semiconductor device of the prior art shown in Fig. 5, a tapered shape is first formed at tip end portions of the inner lead portions 4 of the lead frame 1 by mechanical or chemical working, and the semiconductor chip 3 is then bonded onto the lead frame 1. Thereafter, the semiconductor chip 3 is electrically

connected to the inner lead portions 4 of the lead frame 1 by the thin metal wires 5, and the face of the lead frame 1 for mounting the semiconductor chip 3 is then molded by the sealing resin 6 by means of transfer molding. In order to form external terminals, finally, the outer lead portion 7 of the lead frame 1 which projects from the sealing resin 6 is worked, thereby completing the resin molded type semiconductor device.

In the prior art, in addition to a resin molded type semiconductor device of the structure shown in Fig. 5, also a structure shown in Fig. 6 is employed.

In the resin molded type semiconductor device shown in Fig. 6, an insulative resin tape 8 on which a semiconductor chip 3 is to be mounted is bonded to tip end portions 4a of inner lead portions 4 of a lead frame 1, thereby forming a die pad portion. The device has a structure in which, after the semiconductor chip 3 is mounted on the resin tape 8, terminals of the semiconductor chip 3 are electrically connected to the inner lead portions 4 by thin metal wires 5, and the face of the lead frame 1 for mounting the semiconductor chip 3 is molded by a sealing resin 6. The resin molded type semiconductor device shown in Fig. 6 has the merit that the device can be made thinner than the resin molded type semiconductor device shown in Fig. 5. Specifically, in the resin molded type semiconductor device shown in Fig. 6, the resin tape 8 is bonded to the lower faces of the inner lead portions 4 of the lead frame 1 and the

semiconductor chip 3 is mounted on the upper face of the portion. Therefore, the step difference between the upper faces of the inner lead portions 4 and the upper face of the semiconductor chip 3 is reduced. As a result, also the resin thickness of the sealing resin 6 is reduced, and the resulting resin molded type semiconductor device has a reduced thickness. In the resin molded type semiconductor device shown in Fig. 5, since the semiconductor chip 3 is mounted on the die pad portion 2 which is in the same level as the inner lead portions 4, the thickness of the sealing resin 6 cannot be reduced by such a degree that is attained in the resin molded type semiconductor device shown in Fig. 6.

In order to realize thinning, however, a resin molded type semiconductor device of the prior art has a structure in which substantially only the face of a lead frame on which a semiconductor chip is mounted, i.e., the upper face of the lead frame is molded by a sealing resin. Even when a tapered shape is formed in an inner lead portion, therefore, the contact area between the lead frame and the sealing resin is reduced as a whole, thereby producing a problem in that the adhesiveness is impaired and the reliability of a product is lowered. Since such a device has a structure in which substantially only the single face of the lead frame is resin-molded, there are further problems in that the semiconductor chip is adversely affected by stress of the sealing resin, and that package crack occurs in the sealing

resin. When the inner lead portions are connected to the semiconductor chip by thin metal wires and single-side molding is performed, there arises a further problem in that, because of stress in the single-side molding structure, a load due to the stress acts on the inner lead portions which are connected by thin metal wires, and the connecting portions are broken, with the result that a connection failure occurs.

Therefore, it is an object of the invention to provide a resin molded type semiconductor device which solves the above-discussed problems of the prior art, in which the adhesiveness between a lead frame and a sealing resin is maintained and stable connection between thin metal wires and inner lead portions are enabled, which has high reliability, and in which thinning is realized, and a method of manufacturing the semiconductor device.

Disclosure of Invention

In order to attain the object, the resin molded type semiconductor device of the invention comprises: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of the semiconductor chip to inner lead portions of the lead frame; a sealing resin which seals an outer peripheral region of the semiconductor chip, the region including a thin metal wire region of the upper face of the semiconductor chip, and a lower

region of the die pad portion; and outer lead portions which are arranged in a bottom face region of the sealing resin, and is characterized in that the lead frame is subjected to an upsetting process so that the die pad portion is located at a position higher than the inner lead portions.

In this way, the lead frame is subjected to an upsetting process so that the die pad portion is located at a position higher than the inner lead portions. Therefore, the sealing resin of a thickness corresponding to the step difference of the upsetting exists below the die pad portion, the adhesiveness between the lead frame and the sealing resin can be improved, and the reliability of a product can be maintained. Even when both the faces, or the upper and lower faces of the lead frame are resin-molded, the thickness of the resin of the lower face is equal to a value corresponding to the step difference of the upsetting. Consequently, the thinning can be realized.

Furthermore, the resin molded type semiconductor device of the invention comprises: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of the semiconductor chip to inner lead portions of the lead frame; a sealing resin which seals an outer peripheral region of the semiconductor chip, the region including a thin metal wire region of the upper face of the semiconductor chip; and outer lead portions which are arranged in a bottom face region of the sealing

resin and which are formed to be continuous to the respective inner lead portions, wherein at least one groove portion is formed in a surface of each of the inner lead portions.

In this way, at least one groove portion is formed in the surface of each of the inner lead portions. Therefore, the anchoring effect to the sealing resin can be improved, stress acting on a lead portion of a product, and stress to the thin metal wires can be relaxed, and leads and the thin metal wires can be prevented from peeling off. Consequently, the reliability of a product can be maintained.

Furthermore, the resin molded type semiconductor device of the invention comprises: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of the semiconductor chip to inner lead portions of the lead frame; a sealing resin which seals an outer peripheral region of the semiconductor chip, the region including a thin metal wire region of the upper face of the semiconductor chip; and outer lead portions which are arranged in a bottom face region of the sealing resin and which are formed to be continuous to the respective inner lead portions, and is characterized in that a plurality of groove portions are formed in a surface of each of the inner lead portions, and a connecting portion of the thin metal wire on a side of the inner lead portion is disposed between the groove portions.

In this way, a plurality of groove portions are formed in the surface of each of the inner lead portions, and a connecting portion of the thin metal wire on the side of the inner lead portion is disposed between the groove portions. Therefore, the anchoring effect to the sealing resin can be improved, stress acting on a lead portion of a product, and stress to the thin metal wires can be relaxed, and leads and the thin metal wires can be prevented from peeling off. In this case, stress due to the structure in which the single face of the lead frame is molded by the sealing resin is absorbed by the groove portions, and does not act on an area between the groove portions. Therefore, the connecting portions of the thin metal wires are not broken and stable connection is enabled.

Furthermore, the resin molded type semiconductor device of the invention comprises: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of the semiconductor chip to inner lead portions of the lead frame; a sealing resin which seals an outer peripheral region of the semiconductor chip, the region including a thin metal wire region of the upper face of the semiconductor chip; and outer lead portions which are arranged in a bottom face region of the sealing resin and which are formed to be continuous to the respective inner lead portions, and is characterized in that a widened portion is formed in each of the inner lead portions.

In this way, a widened portion is formed in the inner lead portions. Therefore, the anchoring effect to the sealing resin can be improved, stress acting on a lead portion of a product, and stress to the thin metal wires can be relaxed, and leads and the thin metal wires can be prevented from peeling off. Consequently, the reliability of a product can be maintained.

Furthermore, the resin molded type semiconductor device of the invention comprises: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of the semiconductor chip to inner lead portions of the lead frame; a sealing resin which seals an outer peripheral region of the semiconductor chip, the region including a thin metal wire region of the upper face of the semiconductor chip; and outer lead portions which are arranged in a bottom face region of the sealing resin and which are formed to be continuous to the respective inner lead portions, and is characterized in that a widened portion is formed in each of the inner lead portions and at least one groove portion is formed in a surface.

In this way, a widened portion is formed in each of the inner lead portions and at least one groove portion is formed in the surface. Therefore, the anchoring effect to the sealing resin can be further improved, stress acting on a lead portion of a product, and stress to the thin metal wires can be further relaxed, and the effect of preventing leads and the thin metal wires from

peeling off is enhanced.

Furthermore, the resin molded type semiconductor device of the invention comprises: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of the semiconductor chip to inner lead portions of the lead frame; a sealing resin which seals an outer peripheral region of the semiconductor chip, the region including a thin metal wire region of the upper face of the semiconductor chip; and outer lead portions which are arranged in a bottom face region of the sealing resin and which are formed to be continuous to each of the inner lead portions, and is characterized in that a widened portion is formed in each of the inner lead portions, a plurality of groove portions are formed in a surface, and connecting portions of the thin metal wires on a side of the inner lead portion are disposed between the groove portions.

In this way, a widened portion is formed in each of the inner lead portions, a plurality of groove portions are formed in the surface, and connecting portions of the thin metal wires on a side of the inner lead portion are disposed between the groove portions. Therefore, the anchoring effect to the sealing resin can be further improved, stress acting on a lead portion of a product, and stress to the thin metal wires can be further relaxed, and the effect of preventing leads and the thin metal wires from peeling off is enhanced. In this case, when two or more groove

portions are disposed and the thin metal wires are connected to an area between the groove portions, the effect of absorbing stress can be enhanced. Moreover, stress due to the structure in which the single face of the lead frame is molded by the sealing resin is absorbed by the groove portions, and does not act on an area between the groove portions. Therefore, the connecting portions of the thin metal wires are not broken and stable connection is enabled.

According to the resin molded type semiconductor device of the invention, in the above configuration, exposed faces of the outer lead portions are arranged in a same level as an outer face of the sealing resin. In this way, the exposed faces of the outer lead portions are arranged in the same level as the outer face of the sealing resin. Unlike the prior art, therefore, the outer lead portions can be arranged so as to be embedded in the bottom face portion of the sealing resin, while the outer lead portions project from a side face of the sealing resin. Therefore, the reliability of the outer lead portions serving as external terminals can be improved, and it is possible to provide a resin molded type semiconductor device which is miniaturized by a size corresponding to the nonprojecting structure of the outer lead portions.

Furthermore, the method of manufacturing a resin molded type semiconductor device of the invention comprises the steps of: performing an upsetting process on a lead frame so that a

die pad portion is located at a position higher than inner lead portions; bonding a semiconductor chip to the die pad portion of the lead frame; electrically connecting terminals of the semiconductor chip to the inner lead portions of the lead frame by thin metal wires; sealing an outer peripheral region of the semiconductor chip, thereby forming a sealing resin, the region including a region of an upper face of the semiconductor chip and electrically connected by the thin metal wires, and a lower region of the die pad portion; and shaping outer lead portions of the lead frame so as to be exposed from an outer face of the sealing resin.

In this way, the lead frame is subjected to an upsetting process so that the die pad portion is located at a position higher than the inner lead portions, and the outer peripheral region of the semiconductor chip including the region of the upper face of the semiconductor chip and electrically connected by the thin metal wires, and the lower region of the die pad portion is molded to form the sealing resin. Therefore, the sealing resin of a thickness corresponding to the step difference of the upsetting exists below the die pad portion, the adhesiveness between the lead frame and the sealing resin can be improved, and the reliability of a product can be maintained. Even when both the faces, or the upper and lower faces of the lead frame are resin-molded, the thickness of the resin of the lower face is equal to the thickness of the step difference of the upsetting.

Consequently, the thinning can be realized.

Furthermore, the method of manufacturing a resin molded type semiconductor device of the invention is characterized in that the method comprises the steps of: bonding a semiconductor chip to a lead frame having inner lead portions in each of which a widened portion is disposed and at least one groove portion is formed in a surface; electrically connecting terminals of the semiconductor chip to the inner lead portions of the lead frame by thin metal wires; sealing an outer peripheral region of the semiconductor chip, thereby forming a sealing resin, the region including a region of an upper face of the semiconductor chip and electrically connected by the thin metal wires, and a lower region of the semiconductor chip; and shaping outer lead portions of the lead frame so as to be exposed from an outer face of the sealing resin, and, when the terminals of the semiconductor chip are to be electrically connected to the inner lead portions by the thin metal wires, the connection is performed while connecting portions of the thin metal wires on the side of the inner lead portions are disposed in the vicinity of the groove portion.

In this way, when the terminals of the semiconductor chip are to be electrically connected to the inner lead portions by the thin metal wires, the connection is performed while connecting portions of the thin metal wires on the side of the inner lead portions are disposed in the vicinity of the groove

portion. Therefore, stress due to the structure in which the single face of the lead frame is molded by the sealing resin is absorbed by the groove portion, the connecting portions of the thin metal wires are not broken, and stable connection is enabled. Moreover, the anchoring effect to the sealing resin can be improved, and stress acting on a lead portion of a product can be relaxed by the groove portion, and leads and the thin metal wires can be prevented from peeling off.

Furthermore, the method of manufacturing a resin molded type semiconductor device of the invention is characterized in that the method comprises the steps of: bonding a semiconductor chip to a lead frame having inner lead portions in each of which a widened portion is disposed and a plurality of groove portions are formed in a surface; electrically connecting terminals of the semiconductor chip to the inner lead portions of the lead frame by thin metal wires; sealing an outer peripheral region of the semiconductor chip, thereby forming a sealing resin, the region including a region of an upper face of the semiconductor chip and electrically connected by the thin metal wires, and a lower region of the semiconductor chip; and shaping outer lead portions of the lead frame so as to be exposed from an outer face of the sealing resin, and, when the terminals of the semiconductor chip are to be electrically connected to the inner lead portions by the thin metal wires, the connection is performed while connecting portions of the thin metal wires on

the side of the inner lead portions are disposed between the groove portions.

In this way, when the terminals of the semiconductor chip are to be electrically connected to the inner lead portions by the thin metal wires, the connection is performed while connecting portions of the thin metal wires on the side of the inner lead portions are disposed between the groove portions. Therefore, stress due to the structure in which the single face of the lead frame is molded by the sealing resin is absorbed by the groove portions, and does not act on an area between the groove portions. Consequently, the connecting portions of the thin metal wires are not broken, and stable connection is enabled. In this case, when two or more groove portions are disposed and the thin metal wires are connected to an area between the groove portions, the effect of absorbing stress can be enhanced. Moreover, the anchoring effect to the sealing resin can be further improved, and stress acting on a lead portion of a product can be further relaxed by the plural groove portions, and the effect of preventing leads and the thin metal wires from peeling off is enhanced.

Brief Description of Drawings

Fig. 1 is a section view showing a resin molded type semiconductor device of an embodiment of the invention, Fig. 2 is a plan view showing the resin molded type semiconductor device of the embodiment of the invention, Fig. 3 is an enlarged section

view of main portions of the resin molded type semiconductor device of the embodiment of the invention, Fig. 4(a) is a plan view of an inner lead portion of the resin molded type semiconductor device of the embodiment of the invention, Fig. 4(b) is a left side view, Fig. 4(c) is a front view, Fig. 5 is a section view of a resin molded type semiconductor device of the prior art, and Fig. 6 is a section view showing another example of a resin molded type semiconductor device of the prior art.

Best Mode for Carrying Out the Invention

A resin molded type semiconductor device of an embodiment of the invention will be described with reference to Figs. 1 to 4.

Fig. 1 is a section view of the resin molded type semiconductor device of the embodiment of the invention, Fig. 2 is a plan view of the device, Fig. 3 is an enlarged section view showing an inner lead portion of the device, Fig. 4(a) is an enlarged plan view showing a tip end of the inner lead portion, Fig. 4(b) is a left side view, and Fig. 4(c) is a front view. In Fig. 2, for the sake of convenience, the plan view is a view which is obtained by partially removing away a sealing resin, in order to show the internal structure. In the figure, broken lines show a die pad portion and part of suspension leads.

As shown in Figs. 1 and 2, the resin molded type semiconductor-device comprises: a semiconductor chip 12 which is mounted on a die pad portion 11 of a lead frame 9 and serving

as a supporting portion of the semiconductor chip 12 supported by suspension leads 10; thin metal wires 14 which electrically connect terminals of the upper face of the semiconductor chip 12 to inner lead portions 13 of the lead frame 9; a sealing resin 15 which seals an outer peripheral region of the semiconductor chip 12 including a thin metal wire 14 region of the upper face of the semiconductor chip 12, and a lower region of the die pad portion 11; and outer lead portions 16 which are arranged in a bottom face region of the sealing resin 15, which are formed to be continuous to the respective inner lead portions 13, and which serve as external terminals. The lead frame 9 is subjected to an upsetting process so that the die pad portion 11 is located at a position higher than the inner lead portions 13. In the embodiment, the device is configured so that the die pad portion 11 is smaller in area than the semiconductor chip 12 to be mounted. As described above, in the resin molded type semiconductor device, the suspension leads 10 are subjected to an upsetting process, and a step portion 17 is provided. Therefore, a sealing resin 15a can exist also below the die pad portion 11. Although the device is of the thin type, the device is a semiconductor device which is substantially of the double-side molding type with respect to the lead frame 9.

As shown in Figs. 3 and 4, each of the inner lead portions 13 has a widened portion 18 at a tip end portion, and a plurality of groove portions 19 are formed in the surface. In the end face

of the tip end portion of the inner lead portion 13, a reverse taper is formed in the thickness direction. The outer lead portions 16 are arranged so that their exposed faces are in a substantially same level as a side face portion of the sealing resin 15, and do not protrude from the sealing resin 15 unlike the prior art configuration. Therefore, deformation of the outer lead portions 16, and the like can be prevented from occurring, and the device is a semiconductor device of the surface mount type. Moreover, the connecting portion of each thin metal wire 14 on the side of the inner lead portion 13 are disposed between the groove portions 19.

The resin molded type semiconductor device of the embodiment is a resin molded type semiconductor device which is very thin or has a total thickness of 0.7 [mm], and has a target thickness which is not larger than a sum of the thickness of a semiconductor chip and 1 [mm]. The step difference of the upsetting process of the suspension leads 10 is 0.1 [mm], and the thickness of the sealing resin 15a below the die pad portion 11 is 0.1 [mm]. The thickness of the semiconductor chip 12 is 0.2 [mm], and a sealing resin 15b above the die pad portion 11 is 0.15 [mm].

Next, a method of manufacturing the resin molded type semiconductor device of the embodiment shown in Figs. 1 to 4 will be described.

First, the suspension leads 10 supporting the die pad

portion 11 of the lead frame 9 is pressurized to be subjected to an upsetting process, thereby forming the step portion 17. The semiconductor chip 12 is bonded at the bottom face side to the die pad portion 11 of the lead frame 9 by an electrically conductive adhesive agent.

Next, the terminals of the semiconductor chip 12 on the die pad portion 11 are electrically connected to the inner lead portions 13 of the lead frame 9 by the thin metal wires 14. At this time, each thin metal wire 14 which is to be connected to the side of the corresponding inner lead portion 13 is connected so as to exist between two groove portions 19 which are disposed in the surface of the inner lead portion 13.

Next, the outer peripheral region of the semiconductor chip 12 is molded by the sealing resin 15 by means of transfer molding. In this case, the upper face of the semiconductor chip 12, i.e., the region where electrical connection is done by the thin metal wires 14, and the lower region of the die pad portion 11 are molded, thereby forming the sealing resin 15a and the sealing resin 15b. The thickness of the sealing by the sealing resin 15 is set so that the sealing resin 15a below the die pad portion 11 is flush with the bottom face of the inner lead portion 13 and the sealing resin 15b on the upper face of the semiconductor chip 12 has a thickness which is larger than the loop height of the thin metal wires 14. In the resin sealing step, the sealing must be performed so as to attain excellent air tightness so that the

sealing resin 15 does not enter the bottom region of the inner lead portions 13.

Then, the outer lead portions 16 of the lead frame 9 are shaped so as to be exposed with being flush with the outer face of the sealing resin 15.

As a result of the above-described steps, it is possible to realize a resin molded type semiconductor device of the double-side molding type with respect to the lead frame 9. Because of the double-side molding structure, the adhesiveness between the sealing resin 15 and the lead frame 9 is ensured, and package crack is prevented from occurring, thereby enabling the reliability to be maintained.

Furthermore, by the widened portion 18 and the groove portions 19 which are disposed in the surface of each of the inner lead portions 13, the adhesiveness with the sealing resin 15 can be improved, and stress which acts on the inner lead portions 13 and due to the single-side molding structure can be relaxed, and also the adhesiveness (anchoring effect) with the sealing resin 15 can be improved. In other words, dislocation from the sealing resin 15 to the inner lead portions 13 is prevented from occurring.

With respect to the inner lead portions 13, the sealing resin 15 is formed into the single-side molding structure. According to this structure, therefore, stress by the sealing resin 15 acts on the inner lead portions 13. However, the groove

portions 19 are formed in the inner lead portions 13, and the stress acting on the inner lead portions 13 can be absorbed by the groove portions 19 so as to be relaxed. Since the connecting portions are disposed between the groove portions 19, the connecting portions are not damaged by the stress to be broken.

As described above, according to the embodiment, the suspension leads 10 of the lead frame 9 are subjected to the upsetting process, and the die pad portion 11 is raised to a level higher than the inner lead portions 13. Therefore, the sealing resin 15 of a thickness corresponding to the step difference of the upsetting exists below the die pad portion 11, the adhesiveness between the lead frame 9 and the sealing resin 15 can be improved, and the reliability of a product can be maintained. Unlike the prior art, the outer lead portions 16 are arranged so as to be embedded into the bottom face portion of the sealing resin 15 without projecting from the side face of the sealing resin 15. Therefore, the reliability of the outer lead portions serving as external terminals can be improved, and it is possible to provide a resin molded type semiconductor device which is miniaturized by a size corresponding to the nonprojecting structure of the outer lead portions. Even when both the faces, or the upper and lower faces of the lead frame 9 are resin-molded, the thickness of the resin of the lower face is equal to the thickness of the step difference of the upsetting. Consequently, the thinning can be realized.

Furthermore, the reduction of the area of the die pad portion 11, and the disposition of an opening can enhance the adhesiveness between the sealing resin 15 and the rear face of the semiconductor chip 12, and the reliability can be ensured.

Furthermore, the adhesiveness with the sealing resin can be improved, and stress which acts on the inner lead portions 13 and due to the single-side molding structure can be relaxed by the widened portion 18 and the groove portions 19 which are disposed in the surface of each of the inner lead portions 13. Particularly, the groove portions 19 absorb stress to the connecting portions of the thin metal wires 14 on the side of the inner lead portions 13. Therefore, the connecting portions of the thin metal wires 14 are not affected by stress, breakage of the connecting portions is prevented from occurring, stable connection is enabled, and the reliability of a product can be improved, whereby the reliability of the resin molded type semiconductor device can be improved.

In the embodiment, the number of the groove portions 19 of each of the inner lead portions 13 is two. Alternatively, a single groove portion may be disposed and the thin metal wire may be connected to the vicinity of the groove portion, whereby stress acting on the inner lead portion 13 and that on the thin metal wire can be relaxed. Alternatively, two or more groove portions may be formed, and the thin metal wire may be connected to an area between the groove portions, whereby the effect of

absorbing stress can be enhanced. The groove direction of the groove portions elongates along a side face of the semiconductor device. Alternatively, the groove direction may be set to be any direction such as that which intersects a side face. The groove portions may be formed into a mesh-like shape in which grooves elongate longitudinally and latitudinally. Both the groove portions and the widened portion are disposed. Alternatively, only one of the two kinds of portions may be disposed.

CLAIMS

1. A resin molded type semiconductor device comprising: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of said semiconductor chip to inner lead portions of the lead frame; a sealing resin which seals an outer peripheral region of said semiconductor chip, said region including a thin metal wire region of the upper face of said semiconductor chip, and a lower region of said die pad portion; and outer lead portions which are arranged in a bottom face region of said sealing resin, and characterized in that said lead frame is subjected to an upsetting process so that said die pad portion is located at a position higher than said inner lead portions.

2. A resin molded type semiconductor device comprising: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of said semiconductor chip to inner lead portions of said lead frame; a sealing resin which seals an outer peripheral region of said semiconductor chip, said region including a thin metal wire region of the upper face of said semiconductor chip; and outer lead portions which are arranged in a bottom face region of said sealing resin and which are formed to be continuous to respective inner lead portions, and characterized in that at least one groove portion is formed in a surface of each of said inner lead portions.

3. A resin molded type semiconductor device comprising: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of said semiconductor chip to inner lead portions of said lead frame; a sealing resin which seals an outer peripheral region of said semiconductor chip, said region including a thin metal wire region of the upper face of said semiconductor chip; and outer lead portions which are arranged in a bottom face region of said sealing resin and which are formed to be continuous to respective inner lead portions, and characterized in that a plurality of groove portions are formed in a surface of each of said inner lead portions, and a connecting portion of said thin metal wire on a side of said inner lead portion is disposed between said groove portions.

4. A resin molded type semiconductor device comprising: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of said semiconductor chip to inner lead portions of said lead frame; a sealing resin which seals an outer peripheral region of said semiconductor chip, said region including a thin metal wire region of the upper face of said semiconductor chip; and outer lead portions which are arranged in a bottom face region of said sealing resin and which are formed to be continuous to respective inner lead portions, and characterized in that a widened portion is formed in each

of said inner lead portions.

5. A resin molded type semiconductor device comprising: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of said semiconductor chip to inner lead portions of said lead frame; a sealing resin which seals an outer peripheral region of said semiconductor chip, said region including a thin metal wire region of the upper face of said semiconductor chip; and outer lead portions which are arranged in a bottom face region of said sealing resin and which are formed to be continuous to respective inner lead portions, and characterized in that a widened portion is formed in each of said inner lead portions and at least one groove portion is formed in a surface.

6. A resin molded type semiconductor device comprising: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of said semiconductor chip to inner lead portions of said lead frame; a sealing resin which seals an outer peripheral region of said semiconductor chip, said region including a thin metal wire region of the upper face of said semiconductor chip; and outer lead portions which are arranged in a bottom face region of said sealing resin and which are formed to be continuous to respective inner lead portions, and characterized in that a widened portion is formed in each

of said inner lead portions, a plurality of groove portions are formed in a surface, and connecting portions of said thin metal wires on a side of said inner lead portion are disposed between said groove portions.

7. A resin molded type semiconductor device according to claim 1, 2, 3, 4, 5, or 6, wherein exposed faces of said outer lead portion are arranged in a same level as an outer face of said sealing resin.

8. A method of manufacturing a resin molded type semiconductor device comprising the steps of: performing an upsetting process on a lead frame so that a die pad portion is located at a position higher than inner lead portions; bonding a semiconductor chip to said die pad portion of said lead frame; electrically connecting terminals of said semiconductor chip to said inner lead portions of said lead frame by thin metal wires; sealing an outer peripheral region of said semiconductor chip, thereby forming a sealing resin, said region including a region of an upper face of said semiconductor chip and electrically connected by said thin metal wires, and a lower region of said die pad portion; and shaping outer lead portions of the lead frame so as to be exposed from an outer face of said sealing resin.

9. A method of manufacturing a resin molded type semiconductor device characterized in that said method comprises the steps of: bonding a semiconductor chip to a lead frame having inner lead portions in each of which a widened portion is disposed and at

least one groove portion is formed in a surface; electrically connecting terminals of said semiconductor chip to said inner lead portions of said lead frame by thin metal wires; sealing an outer peripheral region of said semiconductor chip, thereby forming a sealing resin, said region including a region of an upper face of said semiconductor chip and electrically connected by said thin metal wires, and a lower region of said semiconductor chip; and shaping outer lead portions of said lead frame so as to be exposed from an outer face of said sealing resin, and, when said terminals of said semiconductor chip are to be electrically connected to said inner lead portions by said thin metal wires, the connection is performed while connecting portions of said thin metal wires on the side of said inner lead portions are disposed in the vicinity of said groove portion.

10. A method of manufacturing a resin molded type semiconductor device characterized in that said method comprises the steps of: bonding a semiconductor chip to a lead frame having inner lead portions in each of which a widened portion is disposed and a plurality of groove portions are formed in a surface; electrically connecting terminals of said semiconductor chip to said inner lead portions of said lead frame by thin metal wires; sealing an outer peripheral region of said semiconductor chip, thereby forming a sealing resin, said region including a region of an upper face of said semiconductor chip and electrically connected by said thin metal wires, and a lower region of said

semiconductor chip; and shaping outer lead portions of said lead frame so as to be exposed from an outer face of said sealing resin, and, when said terminals of said semiconductor chip are to be electrically connected to said inner lead portions by said thin metal wires, the connection is performed while connecting portions of said thin metal wires on the side of said inner lead portions are disposed between said groove portions.

Fig. 1

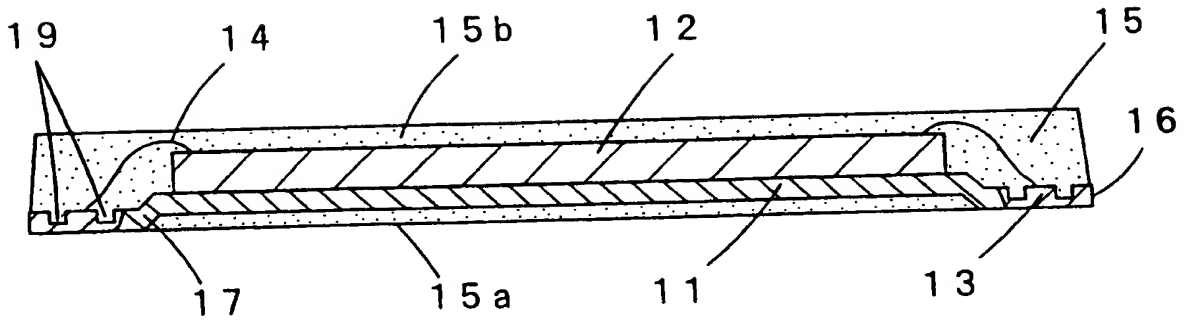


Fig. 2

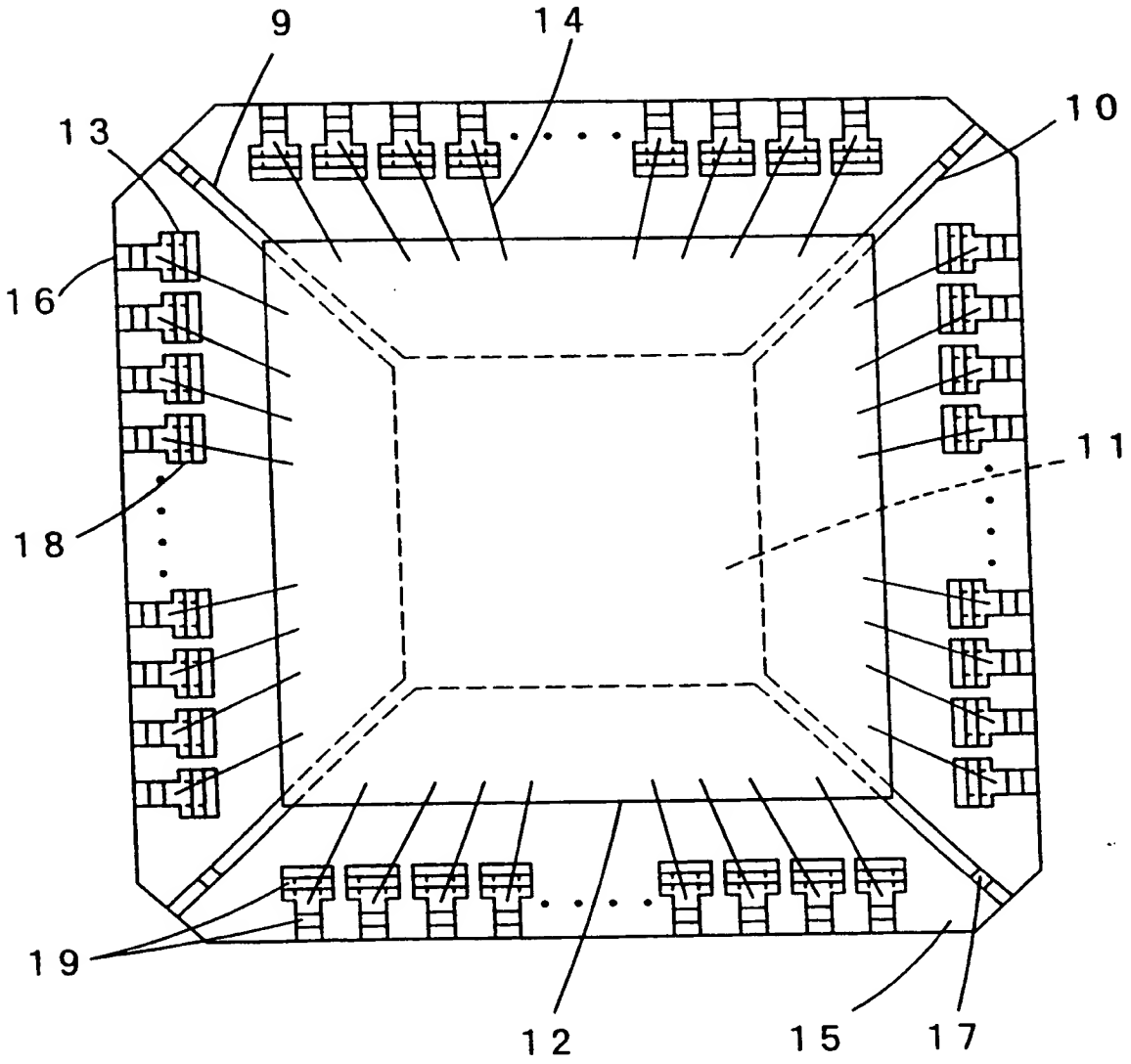


Fig. 3

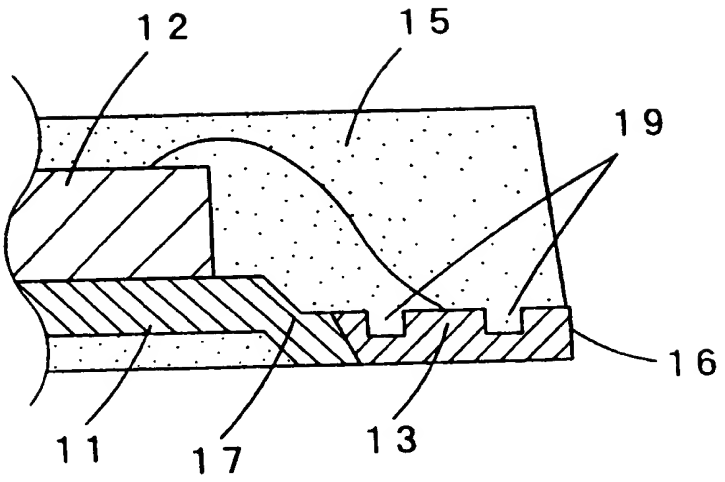


Fig. 4

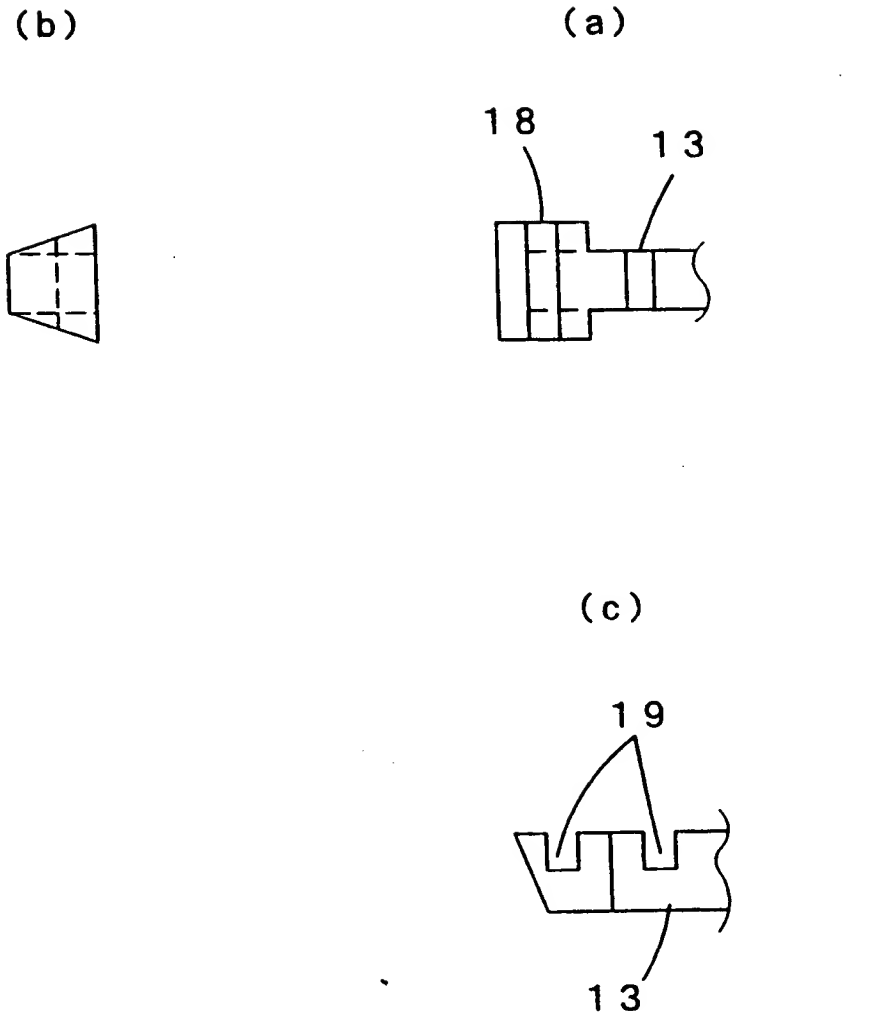


Fig. 5

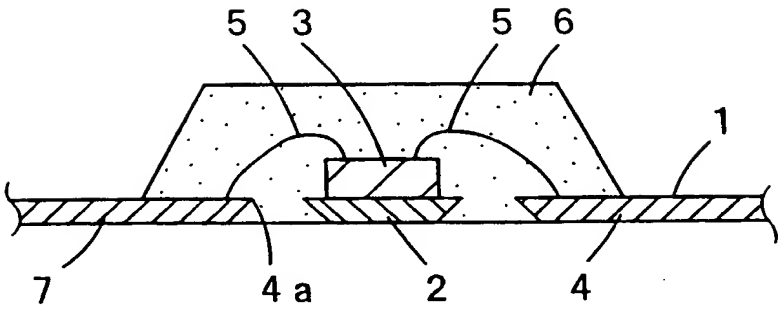
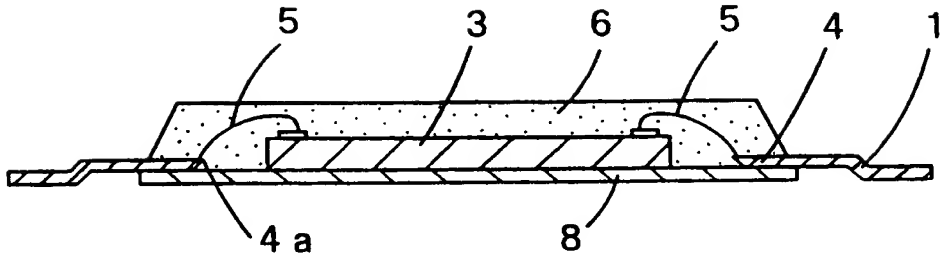


Fig. 6



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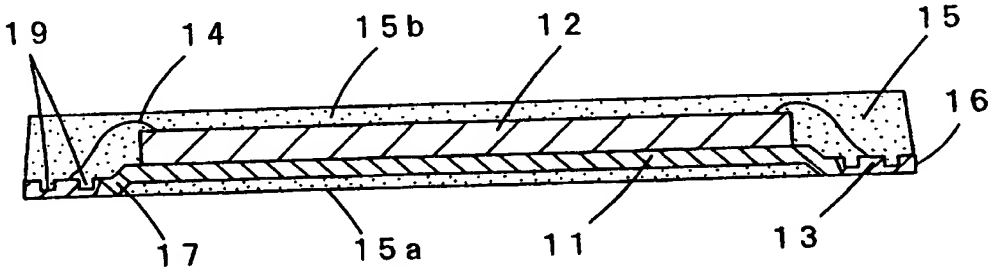

(57) Abstract

A resin molded type semiconductor device has: a semiconductor chip (12) which is mounted on a die pad portion (11) of a lead frame (9); thin metal wires (14) which connect terminals of the semiconductor chip (12) to inner lead portions (13) of the lead frame (9); and a sealing resin (15), and the lead frame (9) is subjected to an upsetting process so that a supporting portion (11) is located at a position higher than the inner lead portions (13). Since the sealing resin of a thickness corresponding to the step difference of the upsetting exists below the supporting portion, the adhesiveness between the lead frame and the sealing resin can be improved, and high reliability and thinning are realized. Since at least one groove portion is disposed in the surface of each of the inner lead portions (13), the anchoring effect to the sealing resin (15), stress acting on a lead portion of a product, and stress to the thin metal wires (14) can be relaxed, and leads and the thin metal wires can be prevented from peeling off.

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 98/02544

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/31

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 009, no. 230 (E-343), 17 September 1985 -& JP 60 086851 A (NIPPON DENKI KK), 16 May 1985 see abstract; figures 3,5	1,7,8
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 307 (E-1229), 7 July 1992 -& JP 04 085952 A (FUJITSU LTD), 18 March 1992 see abstract; figures 1-4	1,7,8

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[X] Further documents are listed in the continuation of box C. [ ] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 February 1999	19. 03. 1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Zeisler, P

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 98/02544

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 489 (E-0994), 24 October 1990 -& JP 02 201946 A (NEC IC MICROCOMPUT SYST LTD), 10 August 1990 see abstract	1,7,8
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 078 (E-718), 22 February 1989 -& JP 63 258050 A (MITSUBISHI ELECTRIC CORP), 25 October 1988	1
A	see abstract	8
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 346 (E-798), 3 August 1989 -& JP 01 106456 A (MATSUSHITA ELECTRIC IND CO LTD), 24 April 1989	4,5,9
A	see abstract; figures 1-3	10
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 346 (E-798), 3 August 1989 -& JP 01 106455 A (MATSUSHITA ELECTRIC IND CO LTD), 24 April 1989	2
A	see abstract; figure 1	9
X	PATENT ABSTRACTS OF JAPAN vol. 017, no. 504 (E-1430), 10 September 1993 -& JP 05 129473 A (SONY CORP), 25 May 1993	3
A	see abstract; figures 5C,5D	9,10
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 287 (E-643), 5 August 1988 -& JP 63 064351 A (TOSHIBA CORP), 22 March 1988 see abstract	2,3,5,6, 9,10
A	PATENT ABSTRACTS OF JAPAN vol. 010, no. 137 (E-405), 21 May 1986 -& JP 61 001042 A (TOSHIBA KK), 7 January 1986 see abstract	2,3,5,9, 10
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 444 (E-1265), 16 September 1992 -& JP 04 155854 A (HITACHI LTD;OTHERS: 01), 28 May 1992 see abstract	3,6,10

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP 98/02544

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

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Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1,7,8

   Resin molded type semiconductor device with die pad located higher than inner lead portions

2. Claims: 2,3,9

   Resin molded type semiconductor device with groove portion(s) in inner lead portions

3. Claims: 4,5,6,10

   Resin molded type semiconductor device with widened inner lead portions